

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the applications:

Listing of Claims:

1. (Currently Amended) An integrated circuit, comprising:
a substrate;
a plurality of metal layers, a first metal layer of said plurality of metal layers
being disposed on said substrate;
an inductor layer disposed within said plurality of metal layers; and
a circuitry for generating a negative capacitance, said circuitry comprising:
at least two transistors;
at least two resistors; each resistor of said at least two resistors being
coupled to each of said at least two transistors; and
a capacitor coupled to a first transistor of said at least two transistors and a
first resistor of said at least two resistors;
wherein said circuitry generates ~~generating~~ said negative capacitance of a value to
compensate for a capacitance associated with metal layers adjacent to said inductor layer,
said circuitry being coupled to said inductor layer.
2. (Original) The integrated circuit as claimed in claim 1, wherein a value of
said negative capacitance is approximately equal in magnitude to said capacitance
associated with metal layers adjacent to said inductor layer.
3. (Canceled)
4. (Currently Amended) The integrated circuit as claimed in claim 1 [[3]],
wherein said at least two transistors are at least one of bipolar transistors, MOSFETS, and
gallium arsenide pseudomorphic high-electron mobility transistors.

5. (Currently Amended) The integrated circuit as claimed in claim 1 [[3]], wherein said negative capacitance generated by said circuitry is dependent upon component values of said at least two resistors and said capacitor.

6. (Original) The integrated circuit as claimed in claim 1, wherein said circuitry is fabricated within the substrate.

7-20. (Canceled)

21. (New) An integrated circuit, comprising:
a substrate;
a plurality of metal layers, a first metal layer of said plurality of metal layers being disposed on said substrate;
an inductor layer disposed within said plurality of metal layers;
a circuitry for generating a negative capacitance fabricated within said substrate, said circuitry comprising:
at least two transistors;
at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors; and
a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors; and
a via coupling said circuitry to said inductor layer,
wherein said circuitry generates said negative capacitance of a value to compensate for a capacitance associated with metal layers adjacent to said inductor layer, said value of said negative capacitance being approximately equal in magnitude to said capacitance associated with metal layers adjacent to said inductor layer.

22. (New) An integrated circuit, comprising:
a substrate;
a plurality of metal layers, a first metal layer of said plurality of metal layers
being disposed on said substrate;
an inductor layer disposed within said plurality of metal layers;
a circuitry for generating a negative capacitance, said circuitry comprising:
at least two transistors;
at least two resistors; each resistor of said at least two resistors being
coupled to each of said at least two transistors; and
a capacitor coupled to a first transistor of said at least two transistors and a
first resistor of said at least two resistors; and
a via coupling said circuitry to said inductor layer,
wherein said circuitry generates said negative capacitance of a value to
compensate for a capacitance associated with metal layers adjacent to said
inductor layer, said value of said negative capacitance being approximately equal
in magnitude to said capacitance associated with metal layers adjacent to said
inductor layer.